CLAIMS

What is claimed is:

1   1.   An apparatus comprising:
2   a first differential output driver to provide a single ended output voltage in
3   response to an input voltage;
4   a second differential output driver to provide a single ended output in
5   response to the input voltage, the first output voltage and the second output voltage
6   representative of the positive and inverted input voltage; and
7   a feedback circuit to monitor the first and second output voltages and apply a
8   bias voltage to at least one of the first and second output drivers to vary the point
9   where the first and second output voltages cross-over as the input voltage changes
10   from a first to a second level.

1   2.   The apparatus of claim 1, wherein the correcting bias voltage forces the first
2   and second output voltages to cross-over at a point substantially equidistant between
3   maximum and minimum output voltages of the first and second differential drivers.

1   3.   The apparatus of claim 1, wherein the first and second output drivers are
2   connected to provide positive and negative outputs to positive and negative
3   conductors of a transmission cable.

1   4.   The apparatus of claim 2, wherein the feedback circuit further includes at
2   least one capacitor, and wherein the feedback circuit places a charge proportional to
3   a difference between an actual cross-over voltage of the first and second output
4   drivers and the equidistant cross-over voltage onto the capacitor to convert the
5   charge into the correcting voltage.

1   5.   The apparatus of claim 4, wherein the at least one capacitor includes a first

2   and second capacitor, wherein the feedback circuit places a charge proportional to a

3   difference between the actual cross-over voltage and the equidistant cross-over

4   voltage onto the first and second capacitors, and wherein the first capacitor supplies

5   a correcting voltage to at least one pull-up bias circuit in the output drivers, and the

6   second capacitor supplies a correcting voltage to at least one pull down bias circuit

7   in the output drivers.

1   6.   The apparatus of claim 5, wherein the feedback circuit applies the correcting

2   voltage to increase a drive strength of the pull-up bias circuit and/or to decrease a

3   drive strength of the pull-down bias circuit if the actual cross-over voltage is lower

4   than the equidistant cross-over voltage.

1   7.   The apparatus of claim 5, wherein the feedback circuit applies the correcting

2   voltage to decrease a drive strength of the pull-up bias circuit and/or to increase the

3   pull-down bias circuit if the cross-over voltage is higher than the equidistant cross-

4   over voltage.

1   8.   The apparatus of claim 4, wherein the first capacitor provides a correcting

2   voltage to a gate of a PMOS transistor in the pull-up bias circuit, and wherein the

3   second capacitor provides a correcting voltage to a gate of an NMOS transistor in

4   the pull-down bias circuit.

1   9.   The apparatus of claim 5, further including:

2   a differential receiver for detecting a cross-over voltage transition on the

3   differential interface, the differential receiver having a first output;

4   a single-ended receiver for detecting rail-to-rail transitions on the positive

5   conductor, the receiver for the positive conductor having a second output;

6   a single-ended receiver for detecting rail-to-rail transitions on the negative

7   conductor, the receiver for the negative conductor having a third output; and

8   wherein if the cross-over voltage is lower than the equidistant voltage,

9   charge on the first capacitor is reduced while the first output is high and the second

10   output is low and/or charge on the second capacitor is reduced while the first output

11   is low and the third output is low.

1   10.   The apparatus of claim 9,

2   wherein if the cross-over voltage is higher than the equidistant voltage,

3   charge on the first capacitor is increased while the first output is low and the second

4   output is high and/or charge on the second capacitor is increased while the first

5   output is high and the third output is high.

1   11.   The apparatus of claim 9, wherein the outputs enable switches to apply a

2   high voltage level to the first and second capacitors to increase the charge, and to

3   apply a low voltage level to the first and second capacitors to reduce the charge.

1   12.   The apparatus of claim 11, wherein the switches include transmission-gate

2   switches.

1   13.   The apparatus of claim 1, wherein the transceiver circuit is an interface to a

2   universal serial bus (USB).

1   14.   A method comprising:

2   measuring a difference between a voltage at which output voltage signals of

3   first and second drivers of a differential signal transceiver cross-over and a voltage

4   point substantially equidistant between maximum and minimum output voltages;

5   providing a correcting bias voltage proportional to a difference between the

6   cross-over voltage and the equidistant voltage; and

7   applying the correcting bias voltage to the differential drivers to vary the

8   voltage point where the first and second output voltages cross-over.

1 15. The method of claim 14, wherein providing a correcting bias voltage

2 includes:

3 producing a net charge on at least one capacitor in proportion to the

4 difference between the cross-over voltage and the equidistant voltage; and

5 converting the charge into a correcting bias voltage.

1 16. The method of claim 14, wherein applying the correcting bias voltage to the

2 differential drivers includes feeding back the correcting voltage to the drivers to

3 adjust a drive strength of pull-up and pull-down bias circuits.

1 17. The method of claim 16, wherein adjusting the drive strength of pull-up and

2 pull-down circuit biasing includes:

3 increasing the drive strength of the pull-up bias circuit and/or decreasing the

4 drive strength of the pull-down bias circuit if the cross-over voltage is lower than

5 the equidistant voltage; and

6 decreasing the drive strength of the pull-up bias circuit and/or increasing the

7 drive strength of the pull-down bias circuit if the cross-over voltage is higher than

8 the equidistant voltage.

1 18. The method of claim 17, wherein

2 increasing the drive strength of the pull-up bias circuit includes decreasing a

3 gate voltage on a PMOS transistor,

4 decreasing the drive strength of the pull-up bias circuit includes increasing a

5 gate voltage of the PMOS transistor,

6 increasing a drive strength of the pull-down bias circuit includes increasing a

7 gate voltage on an NMOS transistor, and

8 decreasing the drive strength of the pull-down bias circuit includes decreasing a gate

9 voltage on the NMOS transistor.

1   19.   The method of claim 15, wherein the net charge produced is zero when the

2   cross-over voltage matches the equidistant voltage.

1   20.   The method of claim 15, wherein the at least one capacitor includes a first

2   and second capacitor and producing a charge on a capacitor includes switching a

3   power supply rail onto the first and second capacitor.

1   21.   The method of claim 20, wherein adjusting a pull-up circuit bias includes

2   applying a correcting voltage on the first capacitor to adjust a pull-up bias voltage,

3   and adjusting a pull-down circuit bias includes applying a correcting voltage on the

4   second capacitor to adjust a pull-down capacitor voltage.

1   22.   The method of claim 15, wherein measuring further includes:

2   measuring a cross-over transition on positive and negative conductors of a

3   transmission cable with the differential signal transceiver;

4   measuring a rail-to-rail transition on the positive conductor of the

5   transmission cable;

6   measuring a rail-to-rail transition on the negative conductor of the

7   transmission cable; and

8   wherein producing a net charge includes switching a charge onto the

9   capacitor when there is a mismatch in transition times.

1   23.   The method of claim 22, wherein measuring further includes:

2   providing a single ended output transition on a differential receiver in

3   response to the cross-over transition;

4   providing a single ended output transition on an output of a first single ended

5   receiver in response to a transition exceeding a first voltage threshold on the

6   positive conductor; and

7   providing a single ended output transition on an output of a second single

8   ended receiver in response to a transition exceeding a second voltage threshold on

9   the negative conductor.

1   24.   The method of claim 23, wherein providing the single ended output

2   transition of the differential receiver includes providing a transition that follows the

3   transition on the positive conductor, and wherein switching includes:

4   a) switching a low supply onto the first capacitor while an output of the

5   differential receiver is at a high voltage and an output of the first single-ended

6   receiver is at a low voltage;

7   b) switching a high supply onto the first capacitor while the output of the

8   differential receiver is at a low voltage and the output of the first single-ended

9   receiver is at a high voltage;

10   c) switching a low supply onto the second capacitor while the output of the

11   differential receiver is at a low voltage and an output of the second single-ended

12   receiver is at a low voltage; and

13   d) switching a high supply onto the second capacitor while the output of the

14   differential receiver is at a high voltage and the output of the second single-ended

15   receiver is at a high voltage.

1   25.   A system comprising:

2   a transceiver interface coupled to a differential communication bus, the

3   transceiver interface having a differential cross-over voltage of a magnitude

4   between high and low transceiver output voltages;

5   a transceiver controller in communication with the transceiver interface; and

6   a cross-over lock feedback circuit to correct deviations of the cross-over

7   voltage from a voltage point equidistant between maximum and minimum output

8   voltages of the transceiver.

1   26.   The system of claim 25, wherein the transceiver interface further includes at

2   least one transceiver driver coupled to the cross-over lock feedback circuit, the

3   driver having pull-up and pull-down circuits; and wherein the feedback circuit feeds

4   back a correcting voltage to the driver to adjust the pull-up and/or pull-down of the

5   driver to correct the cross-over voltage.

1   27.   The system of claim 26, wherein the cross-over lock feedback circuit

2   produces a charge in proportion to a difference of the cross-over voltage from the

3   equidistant voltage to provide the correcting voltage.

1   28.   The system of claim 27, wherein the transceiver interface further includes:

2   a differential receiver;

3   a single-ended receiver coupled to a positive node on the differential bus;

4   and

5   a single-ended receiver coupled to a negative node on the differential bus,

6   wherein the feedback circuit produces a charge based on asymmetry of

7   switching times at receiver outputs when the cross-over voltage is different from the

8   midpoint voltage.

1   29.   A system comprising:

2   a transceiver interface coupled to a differential communication bus, the

3   transceiver interface having a differential cross-over voltage of a magnitude

4   between high and low transceiver output voltages;

5   a transceiver controller in communication with the transceiver interface; and

6   a cross-over lock feedback circuit to correct deviations of the cross-over

7   voltage from a voltage point equidistant between maximum and minimum output

8   voltages of the transceiver;

9   a processor in communication with the transceiver controller; and

10   a DRAM memory in communication with the processor.

1   30.   The system of claim 29, wherein the transceiver interface further includes at
2   least one transceiver driver coupled to the cross-over lock feedback circuit, the
3   driver having pull-up and pull-down circuits; and wherein the feedback circuit feeds
4   back a correcting voltage to the driver to adjust the pull-up and/or pull-down of the
5   driver to correct the cross-over voltage.

1   31.   The system of claim 30, wherein the cross-over lock feedback circuit
2   produces a charge in proportion to a difference of the cross-over voltage from the
3   equidistant voltage to provide the correcting voltage.